ABSTRACT OF THE DISCLOSURE

A semiconductor device and a manufacturing method thereof are obtained which can restrain increase of the parasitic capacitance generated between contact plugs of source/drain regions and a gate electrode while reducing the area of the source/drain regions. A channel region is formed under a gate electrode 1. A pair of source/drain regions 2 are formed to sandwich the channel region. The source/drain regions 2 have a first part 3a being adjacent to the channel region and a second part 3b formed to protrude in a channel width direction from the first part 3a so that a part of outer peripheries of the source/drain regions 2 extend away from the gate electrode 1 in a plan view. Contact plugs 4 are formed on the second part 3b for connecting the source/drain regions 2 to source/drain wirings.